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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,936	08/27/2003	George M. Braceras	BUR920020100US1	1935

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,936	BRACERAS ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8-10,12 and 17* is/are rejected.

7)☒ Claim(s) *2-4,7,11,13-16 and 18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 6, 8-10, 12 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jang et al. (U. S. PAT. 6,762,620).

In claim 1, Jang et al. teaches all claimed features in col. 2, lines 10-67, a memory system comprising: a scalable termination circuit (multiple modes of termination, line 12) having: a first resistive element (line 66) coupled to a first port (output terminal); a second resistive element (PM1 in Fig. 5) coupled to a second port (second output terminal); a first logic circuit (a logic circuit that produces a plurality of binary bits, line 63) coupled to the first and second resistive elements, and adapted to determine a characteristic impedance (preprogrammed value) of the first port by generating a plurality of binary termination signals; and a second logic circuit (100) coupled to the first logic circuit (for receiving binary bits CONP1-CONPn) and the second resistive element, and adapted to modify (a characteristic impedance (variable value) of the second port by manipulating one or more of the plurality of binary termination signals (CONP1-CONPn).

In claim 5, Jang et al. further teaches the memory system of claim 1 wherein the second logic circuit is further adapted to modify the characteristic impedance of the second port by manipulating one or more of the plurality of binary termination signals by performing at east one of a multiplication (counters 150, 152 in Fig. 5) and division operation on the binary termination signals.

In claim 6, Jang et al. further teaches the memory system of claim 1 wherein the first and second resistive elements includes a plurality of stacked transistor pairs (bank of resistors; col. 2, line 64) connected in parallel.

In claim 8, Jang et al. teaches all claimed features in col. 2, lines 10-30, a method of providing multiple termination values (line 12) using a plurality of binary termination signals (line 63) comprising: determining a characteristic impedance (preprogrammed, line 13) of a first port (input terminal of a selector, line 25) by generating a plurality of binary termination signals (col. 2, line 67); and modifying a characteristic impedance (a variable impedance, line 24) of a second port (a second input terminal for the selector) by manipulating one or more of the plurality of binary termination signals.

In claim 9, Jang et al. further teaches the method of claim 8 wherein modifying the characteristic impedance of the second port includes modifying the characteristic impedance of the second port by manipulating one or more of the plurality of binary termination signals by performing at east one of a multiplication (counters 150, 152 in Fig. 5) and division operation.

In claim 10, Jang et al. further teaches the method of claim 8 further comprising modifying the characteristic impedance of the second port (the second input terminal for the selector) by out-putting control signals (CONP1 in fig. 5) to a resistive element (PM1) coupled to the second port.

Method claim 12 corresponds to detailed method steps al ready discussed similarly with regard to method claim 8.

Apparatus claim 17 corresponds to detailed circuitry already discussed similarly with regard to claim 1.

3. Claims 2-4, 7, 11, 13-16 and 18-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER